Claim 10 was rejected under 35 USC 112, first and second paragraphs, as being non-enabling and indefinite for failing to particularly point out and distinctly claim the subject matter of the invention. Claim 10 has been canceled, and new claim 13 now recites a "low-resistance chip resistor", which type of resistor is well known to those of ordinary skill in the art. Therefore, it is believed that claim 13 overcomes the rejections under 35 USC 112.

As recited in claim 6, Applicant claims a BGA (ball grid array) package, including: a plurality of continuous electrically-conductive traces for electrically connecting a first subgroup of bond fingers to corresponding vias, the traces including at least one trace interposed between a second subgroup of bond fingers and their corresponding vias; and an electrically-conductive bridge as a bonding wire that spans in an overhead manner across the interposing electrically-conductive trace, such that the bonding wire is free of interference with the electrically-conductive trace (see gold wire 90' in FIG. 6).

As recited in claim 11, the electrically-conductive bridge is a chip resistor that spans in an overhead manner across the interposing electrically-conductive trace such that the chip resistor is free of interference with the interposing electrically-conductive trace (see chip resistor 90" in FIG. 7).

The above-described arrangements of an electrically-conductive bridge can yield significant benefits. In the example of FIG. 6, because the gold wire 90' connects the traces by existing wire-bonding technology, it can be implemented in an easy and cost-effective manner. Similarly, in FIG. 7, existing surface-mounting technology (SMT) is used to bond the chip resistor 90" between the traces, thereby bridging the interposing trace without requiring the use of a multi-layer substrate.

Claims 6-10 were rejected under 35 USC 103(a) as being unpatentable over "Applicant's Prior Art Figures 3 and 4" in view of U.S. Patent 3,560,256 to Abrams. This rejection is respectfully traversed.

As discussed in the background section of the specification, prior art FIG. 3 describes an example where bond finger 60B cannot be connected to the via 80A by using a continuous electrically-conductive trace (see page 3, lines 2-3), without impacting the interposing trace 70A. Prior art FIG. 4 provides a solution to the problem illustrated in FIG. 3 by incorporating a multi-layer substrate; however, the Applicant's specification expressly teaches away from the use of a multi-layer substrate due to its high cost and complexity (see page 3, first full paragraph).

Abrams fails to teach or suggest an electrically-conductive bridge as either a bonding wire or a chip resistor which spans an interposing trace and is free of interference with the interposing trace. In Abrams, a thick and thin-film circuit includes at least three glazed conductors, a glazed dielectric formed over one of the conductors, and a thin-film crossover resistor formed over the dielectric and connected to the other conductor. Neither the thin-film crossover resistor 28 nor the crossover conductor 26 taught in Abrams are equivalent to the "bonding wire" or "chip resistor" recited in the Applicant's claimed invention, as the circuit of Abrams cannot be formed by the simple wire-bonding and SMT processes taught in the Applicant's invention. In contrast, the connecting structures taught in Abrams are formed by different manufacturing steps that are expensive and time-consuming.

There is no teaching or suggestion of providing an electrically-conductive bridge as either a bonding wire or chip resistor, as taught in the Applicant's claimed invention. It is unclear how Abrams could be combined with prior art FIGS. 3 or 4 to produce the Applicant's invention.

The other references cited in the Office Action fail to teach or suggest the use of a bonding wire or a chip resistor as an electrically-conductive bridge which spans an interposing trace and is free of interference with the interposing trace. For example, U.S. Patent 3,801,388 to Akiyama et al. discloses a printed circuit board in which parts of leads are crossed over without being electrically connected with one another, by means of forming first and second conductive layers on opposite sides of a conductive substrate, the material of the first and second layers having a different etching characteristic than the substrate material, and then etching the first and

second layers. The printed circuit board structure of Akiyama et al. is produced by a manufacturing process having expensive, time consuming steps. U.S. Patent 5,473,196 to De Givry discloses a large capacity memory component enabling a plurality of components to be stacked while keeping open the option of connection to an interconnection support. U.S. Patent 6,013,573 to Yagi discloses an air bridge type shape that joins to a substrate or micro-structure manufactured by forming an air bridge type structure on a first substrate and transferring the air bridge type structure to a second substrate and/or a micro-structure formed on the second substrate. The air bridge type structure of Yagi requires relatively expensive, time consuming steps in the manufacturing process. None of the above references teach or suggest the use of a bonding wire or chip resistor as an electrically-conductive bridge which spans an interposing trace, or where such a bridge can be formed by simple wire-bonding or SMT processes taught in the Applicant's invention.

It is believed the application is in condition for immediate allowance, which action is earnestly solicited.



Respectfully submitted,

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APPENDIX A:
VERSION WITH MARKINGS TO SHOW CHANGES MADE

The title has been canceled and replaced with the following new title:

BALL GRID ARRAY PACKAGE WITH ELECTRICALLY-CONDUCTIVE BRIDGE

IN THE CLAIMS

Claims 6-8 have been amended as follows:

6. (Amended) A BGA (ball grid array) package, which comprises:

(a) a substrate having a front side and a back side;

(b) a semiconductor chip mounted on the front side of the substrate[;], the semiconductor chip having an array of bond pads;

(c) an array of solder balls implanted on the back side of the substrate;

(d) an array of bond fingers provided beside the semiconductor chip and which are electrically connected to the bond pads on the semiconductor chip;

(e) an array of electrically-conductive vias, each penetrating from the front side to the back side of the substrate and electrically connected to one of the solder balls;

(f) a plurality of continuous electrically-conductive traces for electrically connecting a first subgroup of the bond fingers to corresponding ones of the vias[;], these continuous electrically-conductive traces including at least one being interposed between a second subgroup of the bond fingers and their corresponding vias; and

(g) an electrically-conductive bridge [which] as a bonding wire that spans in an overhead manner across [each] the interposing electrically-conductive trace [and having] such that the bonding wire is free of interference with the interposing electrically-conductive trace, wherein the bonding wire has one end electrically connected to the corresponding via and the other end electrically connected to the corresponding bond finger.

7. (Amended) The BGA package of claim 6, wherein the [electrically-conductive bridge is a] bonding wire is mounted through wire-bonding technology.

8. (Amended) The BGA package of claim [7] 6, wherein the bonding wire is a gold wire.

Claims 9 and 10 have been canceled without prejudice or disclaimer.

The following new claims have been added:

11. (New) A BGA (ball grid array) package, which comprises:

(a) a substrate having a front side and a back side;

(b) a semiconductor chip mounted on the front side of the substrate, the semiconductor chip having an array of bond pads;

(c) an array of solder balls implanted on the back side of the substrate;

(d) an array of bond fingers provided beside the semiconductor chip and which are electrically connected to the bond pads on the semiconductor chip;

(e) an array of electrically-conductive vias, each penetrating from the front side to the back side of the substrate and electrically connected to one of the solder balls;

(f) a plurality of continuous electrically-conductive traces for electrically connecting a first subgroup of the bond fingers to corresponding ones of the vias, these continuous electrically-conductive traces including at least one being interposed between a second subgroup of the bond fingers and their corresponding vias; and

(g) an electrically-conductive bridge as a chip resistor that spans in an overhead manner across the interposing electrically-conductive trace such that the chip resistor is free of interference with the interposing electrically-conductive trace, wherein the chip resistor has one end electrically connected to the corresponding via and the other end electrically connected to the corresponding bond finger.

12. (New) The BGA package of claim 11, wherein the chip resistor is mounted through SMT technology.

13. (New) The BGA package of claim 11, wherein the chip resistor is a low-resistance chip resistor.